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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NG, CHRISTINE Y	
ART UNIT	**PAPER NUMBER**
2663	4

DATE MAILED: 06/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/729,531	KAVIPURAPU, GAUTAM NAG	
	Examiner	Art Unit	
	Christine Ng	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-18 and 20* is/are allowed.

6)☒ Claim(s) *1-8,11-13 and 19* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "said second selected port block" in line 9 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 19 recites the limitation "said plurality of pass gates" in lines 2, 4-5 and 7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,210,744 to Yamanaka et al. Yamanaka et al disclose a switch comprising:

A plurality of port blocks (Elements 60-63) comprising a plurality of I/O ports (I0 – I11). Each input-stage cell exchange switch module 60-63 corresponds to respective groups of cell input ports (I0 – I15). Refer to Column 4, lines 8-11 and Abstract.

A plurality of memory cells (Elements 70-73) each including a first pass gate (Header Processing Circuits 9a, 9e...) for coupling a selected line of the first port (Element 60) with a storage element (Memory Circuit 10) and a second pass gate (Header Processing Circuit 9b, 9f...) for coupling a selected line of the second port (Element 61) with the storage element (Memory Circuit 10). Refer to the rejection of claim 1.

A read decoder circuitry (Figure 2, Element 18) for selecting one of the plurality of I/O ports (I0 – I15) of a first selected one of the plurality of port blocks (Elements 60-63) and reading data from a selected memory cell (Memory Circuit 10) of the selected port block. The read enable circuit 18 "gives a read address to each of the memory circuits 10a-10d at a predetermined timing to enable reading of a stored cell (Column 4, lines 48-50), which corresponds to one of the plurality of I/O ports of the port blocks: ports I0 – I3 of port block 60, ports I4 – I7 of port block 61, ports I7 – I11 of port block 62, and ports I12 – I15 of port block 62. Refer to Column 6, lines 12-35 for the method of how the read enable circuit 18 selects which I/O port to read data from.

A write decoder circuitry (Figure 4, Space Switch 4) for selecting one of the plurality of I/O ports (I0 – I15) of a second selected one of the plurality of port blocks (Elements 60-63) and writing data into a selected memory cell (Memory Circuit 10) of the selected port block. Space switch 4 "selects from among the memory circuits 10a-10d memory circuits, from one which has the smallest amount of cells being held therein, and successively write the cells in the selected memory circuits, respectively"

(Column 9, lines 50-57). The space switch writes data in one of the plurality of I/O ports of a selected port block.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,210,744 to Yamanaka et al.

Referring to claim 1, Yamanaka et al disclose in Figure 1 a switching element comprising:

A first port (Element 60) comprising a plurality of lines (I0 – I3); a second port (Element 61) comprising a plurality of lines (I4 – I7); and a third port (Element 62) comprising a plurality of lines (I7 – I11). Each input-stage cell exchange switch module 60-62 corresponds to respective groups of cell input ports (I0 – I11). Refer to Column 4, lines 8-11 and Abstract.

A first memory cell (Element 70) including a storage element (Memory Circuit 10), a first pass gate (Header Processing Circuit 9a) for selectively coupling a first line (F) of the first port (Element 60) to the storage element (Memory Circuit 10), a second pass gate (Header Processing Circuit 9b) for selectively coupling a first line (G) of the second port (Element 61) to the storage element (Memory Circuit 10), and a third pass gate (Header Processing Circuit 9c) for selectively coupling a first line (H) of the third

port (Element 62) to the storage element (Memory Circuit 10). Header processing circuits 9a-9d each "reads and analyzes the destination information of a cell that is outputted from the corresponding cell selecting circuit" (Column 4, lines 29-31) and then outputs the cells to memory circuits 10. The cell selecting circuits "selects and outputs through an address filter a cell which is directed to a specific one of the groups of output ports" (Column 4, lines 23-25). Refer to Column 4, lines 33-38.

A second memory cell (Element 71) including a storage element (Memory Circuit 10), a first pass gate (Header Processing Circuit 9e) for selectively coupling a second line (P) of the first port (Element 60) to the storage element (Memory Circuit 10), a second pass gate (Header Processing Circuit 9f) for selectively coupling a second line (not labeled) of the second port (Element 61) to the storage element (Memory Circuit 10), and a third pass gate (Header Processing Circuit 9g) for selectively coupling a third line (not labeled) of the third port (Element 62) to the storage element (Memory Circuit 10). Header processing circuits 9e-9h operate the same as header processing cuircuits 9a-9d. Refer to Column 5, lines 35-38.

Yamanaka et al disclose four inputs ports instead of three input ports. However, Yamanaka et al disclose "although in the foregoing embodiment...each cell exchange switch module has 4 input ports and 4 output ports, these numbers may be changed as desired" (Column 8, lines 5-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include three input ports instead of four; the motivation being to accommodate other systems that may only need three input ports.

Referring to claim 2, Yamanaka et al disclose that the first (Element 60) and second (Element 61) ports comprise output ports (Elements 80-83) for reading data from the storage elements (Memory Circuits 10) of the memory cells (Element 70) and the third port (Element 62) comprises an input port (Element 7) for writing data to the storage element (Memory Circuits 10) of the memory cells (Element 70). For reading data, all ports (Elements 60-62) have a multiplexer which multiplexes cells that are read out from the memory circuits 10a-10d and directs the cells to specific ones of the groups of output ports (Elements 80-83) depending on their destination. Refer to Column 4, lines 47-61. For writing data, all ports (Elements 60-62) have an input-stage cell multiplexing circuit 7 which multiplexes incoming cells so that they can be sent to a specific one of the groups of output ports through the output-stage cell exchange switch module 70. Refer to Column 4, lines 19-25.

Referring to claim 3, Yamanaka et al disclose that the first (Element 60) and second (Element 61) ports comprise input ports (Elements 80-83) for reading data from the storage elements (Memory Circuits 10) of the memory cells (Element 70) and the third port (Element 62) comprises an output port (Element 7) for writing data to the storage element (Memory Circuits 10) of the memory cells (Element 70). Refer to the rejection of claim 2.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,210,744 to Yamanaka et al in view of U.S. Patent No. 4,237,463 to Bjor et al. Yamanaka et al do not disclose that the storage elements comprise capacitors.

Bjor et al disclose in Figure 16 a memory that is embodied in a capacitor wherein

the "stored values are given by the charges on the capacitors" (Column 5, lines 38-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the storage elements comprise capacitors; the motivation being that data can be written into the capacitor when it is being charged according to a function of its time constant. Capacitors are also commonly used in random access memories with transistors, which act as a switch to selectively read and write data into the capacitor.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,210,744 to Yamanaka et al in view of U.S. Patent No. 5,806,084 to Lin et al. Yamanaka et al do not disclose that the pass gates comprise field effect transistors.

Lin et al disclose that pass gates "electrically couples/decouples a first node to/from a second node under control of signal applied to at least one MOSTFET gate electrode" (Column 5, lines 8-10). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the pass gates comprise field effect transistors; the motivation being that pass gates allow a device to selectively connect to another device based on a signal from the voltage level of a MOSFET. MOSFETs offer the advantage over other field effect transistors in that it offers infinite impedance and is frequently used in high-speed switching applications.

9. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,210,744 to Yamanaka et al in view of U.S. Patent No. 5,365,519 to Kozaki et al.

Referring to claim 7, Yamanaka et al disclose in Figure 2 that the read decoder

(Element 18) selectively couples an output port (K, L, M or N) to a the selected one of the plurality of I/O ports (F, G, H or I) of the first selected port block (Element 60). Refer to Column 6, line 57 to Column 7, line 37.

Yamanaka et al do not disclose that the read decoder comprises a demultiplexer.

Kozaki et al disclose in Figure 2 that the reading process (Element 102) of the switch utilizes a demultiplexer (Element 13). "During the cell read period, the line identifier is outputted from the control table 104 in accordance with the switch unit output port selected by the demultiplexer 13, and the line identifier is used to designate a queue chain to be accessed for reading in the buffer memory 11" (Column 6, lines 18-23). Refer to Column 6, lines 39-61. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include read decoder comprises a demultiplexer; the motivation being that the demultiplexer can separate a plurality of multiplexed data signals that are designated for different destinations with respective destination addresses, thereby allowing the read decoder to determine where in a shared memory to read data designated to one of the multiple destinations.

Referring to claim 8, Yamanaka et al disclose in Figure 2 that the read decoder (Element 18) selectively couples an input port (F, G, H or I) to a the selected one of the plurality of I/O ports (K, L, M or N) of the second selected port block (Element 60). Refer to Column 6, line 57 to Column 7, line 37.

Yamanaka et al do not disclose that the read decoder comprises a multiplexer.

Kozaki et al disclose in Figure 2 that the reading process (Element 102) of the switch utilizes a multiplexer (Element 12). As shown in Figure 3, four streams of data

each arriving at 150 Mbps must be multiplexed into a single stream of data at 600 Mbps in order to accommodate a plurality of different transmission bit rates through a switch. Refer to Column 7, lines 1-26. Data is read from the switch according to a predetermined timing schedule for each output line, which makes it difficult to accommodate a plurality of different types of output lines operating at different transmission rates. Refer to Column 1, lines 51-59. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the read decoder comprises a multiplexer; the motivation being that in order to read data that is leaving a switch at a different bit rate than the operating rate of the switch, the data must be multiplexed together at the receiving end into the rate of the switch and demultiplexed into their original rate at the receiving end; thereby facilitating reading the data from the switch at the predetermined timing schedule.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,210,744 to Yamanaka et al in view of U.S. Patent No. 6,212,181 to Divivier et al. Yamanaka et al do not disclose that the memory cells comprise dynamic random access memory cells.

Divivier et al disclose that modern network devices transfer information by storing cells in a memory cells such as a DRAM, where an arrival engine determines where in the cell memory an arriving cell is stored and a departure engine chooses a cell to retrieve from the cell memory for transmission. Refer to Column 1, lines 13-26. DRAMs are used since any part of the memory can be accessed at any time, rather than having to proceed sequentially through the memory. DRAMs also provide a lot of memory at

low cost, as compared to other RAMs. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the memory cells comprise dynamic random access memory cells; the motivation being that DRAMs are cheaper than other types of RAMs and offer a lot of memory.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,210,744 to Yamanaka et al in view of U.S. Patent No. 5,410,540 to Aiki et al. Yamanaka et al do not disclose that each of the plurality of memory cells of each port block is coupled to a plurality of output I/O ports and an input I/O port.

Aiki et al disclose in Figure 1 a memory cell (Element 4) that is coupled to a plurality of output I/O ports (L91 – L9N) and an input I/O port (one of L01 – L0N). When a broadcast function is required, a cell is received from a certain input I/O port (one of L01 – L0N) and copied to obtain multiple copies through copy section 3 and then sent to memory 4. Refer to Column 4, lines 14-39, "The copies are stored in the memory 4 to be read therefrom according to indication of the output counter 66 and are distributed to t he respective output ports, thereby implementing the broadcast function" (Column 5, lines 24-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each of the plurality of memory cells of each port block is coupled to a plurality of output I/O ports and an input I/O port; the motivation being that it is sometimes necessary for a switch to output an identical cell to a plurality of output ports from a single input port, such as for operations including distribution services and conference services. Refer to Column 1, lines 17-23.

12. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S Patent No. 5,210,744 to Yamanaka et al in view of U.S. Patent No. 6,721,324 Shinohara. Yamanaka et al do not disclose that each of the plurality of memory cells of each port block is coupled to a plurality of input I/O ports and an output port.

Shinohara et al disclose in Figure 26 a memory cell (Element 22) that is coupled to a plurality of input I/O ports (100-1 – 100-n) and an output port (one of 101-1 – 101-n). In a switch, sometimes it may occur that two or more input ports (100-1 – 100-n) will want to send a cell to a specific output port (one of 101-1 – 101-n), thus causing collision; of which only one input port is given connection privilege. Refer to Column 1, lines 23-27 and Column 2, lines 9-15. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each of the plurality of memory cells of each port block is coupled to a plurality of input I/O ports and an output I/O port; the motivation being that cells from different input ports may have the same destination.

Allowable Subject Matter

13. Claims 14-18 and 20 are allowed.

14. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Ng whose telephone number is (703) 305-8395. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Chau can be reached on (703) 308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Ng
May 28, 2004

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